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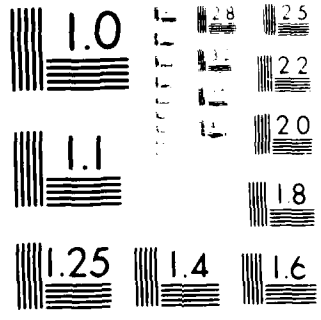
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AD-A189 065

DIGITAL CORRELATOR for the PORTABLE CHANNEL PROBER MEASUREMENT INSTRUMENT

Final Report
December 1987

Contract No. N00014-87-C-2018
(Stow Computer Project NRL02)

Prepared for

Naval Research Laboratory/5550
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This document describes a Digital Correlator for the Portable Channel Prober Measurement Instrument being developed by the Naval Research Laboratory for use in experiments designed to characterize high frequency (HF) radio channels. This Digital Correlator is a digital signal processor designed and constructed by Stow Computer, 111 Old Bolton Road, Stow, MA 01775, (617/508) 897-6838. Two Digital Correlators are integrated into the existing Digital Pre-processor to make a Portable Wideband HF Channel Analyzer. The Portable Wideband HF Channel Analyzer will be located at the receiving site of the channel probing experiment and is situated between the coherent radio receiver and the microcomputer used for data recording and analysis. The Portable Wideband HF Channel Analyzer computes the delay power spectrum of the received waveform. The in-phase and quadrature outputs
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of the receiver are sampled and converted to digital values by the Analog to Digital Converter, integrated by the Integrator, and correlated with a stored replica of the transmitted waveform by two Digital Correlators. The resulting tap gains are then read by the system microcomputer using the microcomputer interface.

The Digital Correlator uses a Texas Instruments TMS320C25 digital signal processor as a central processor and an array of eight Motorola DSP56200 processors to perform the correlation. Input and output is via high-speed dual-port memories. An industry standard VMEbus interface allows the Digital Correlators to be used outside the Portable Wideband HF Channel Analyzer.

The Portable Wideband HF Channel Analyzer is a versatile programmable data acquisition and signal processing system. The Analog to Digital Converters are 12 bits precision and the programmable sampling rate can exceed 250 kHz while sampling both channels simultaneously. The Integrator uses a pair of Texas Instruments TMS32020 digital signal processors for input processing and control. The Digital Correlators are also versatile signal processors and can be used either inside or outside the Portable Wideband HF Channel Analyzer for correlation, digital filtering, fast Fourier transforms (FFT's) and other signal processing applications. The Portable Wideband HF Channel Analyzer is self-contained, weighs about 50 pounds, and is suitable for use on a table top or can be mounted in a standard equipment rack.

DIGITAL CORRELATOR for the PORTABLE CHANNEL PROBER MEASUREMENT INSTRUMENT

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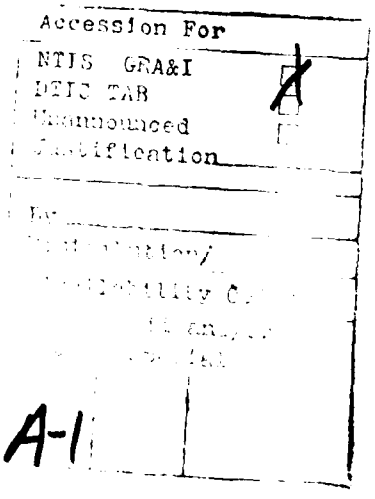

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SECTION 1

Introduction

This document is a final report prepared by Stow Computer of Stow, Massachusetts for the Naval Research Laboratory upon completion of Contract number N00014-87-C-2018 for the design and construction of Digital Correlators for the Portable Channel Prober Measurement Instrument. These Digital Correlators are integrated into the Digital Pre-processor built previously by Stow Computer to form a Portable Wideband HF Channel Analyzer. The Portable Wideband HF Channel Analyzer is a subsystem of the Portable Channel Prober Measurement Instrument being developed by the Naval Research Laboratory for use in experiments designed to characterize high frequency radio communications channels.

The Portable Wideband HF Channel Analyzer is a dual channel data acquisition and processing system comprising analog to digital converters, three signal processors, and a microcomputer interface. The first signal processor is the NRL0101 Integrator built as part of the Digital Pre-processor. The NRL0101 Integrator controls input sampling by the NRL0103 Analog to Digital Converter and can perform integration and other signal processing functions on both data channels simultaneously. The data is then processed by two NRL0201 Digital Correlators, one for each channel. Output from the NRL0201 Digital Correlators is passed to a microcomputer for further analysis and recording. The Portable Wideband HF Channel Analyzer is self-contained, is slightly larger than a personal computer and is suitable for use on a table top or may be mounted in a standard rack.

The Portable Channel Prober Measurement Instrument is used to characterize a wideband high frequency radio channel. A pseudo-noise sequence (PN) sequence is transmitted over the channel. At the receiver site the baseband output of the receiver is processed by the Portable Wideband HF Channel Analyzer. The in-phase and quadrature outputs of the receiver are sampled and converted to digital values. Consecutive sequences of input samples are integrated and the integrated sequences are correlated with a stored replica of the transmitted PN sequence to compute the delay power spectrum of the channel. Correlated values are passed to a general purpose microcomputer for further analysis and storage. Timing and control circuitry maintain synchronization between the transmitting and receiving sites and provide a coherent clock and synchronization signals to the Portable Wideband HF Channel Analyzer.

The current experiment uses two different PN sequences. The Sounder mode uses a 255 bit sequence and is used to make

a preliminary characterization of the channel. The transmitted pulse width is 8 usec with a 25% duty cycle. The received waveform is sampled at 32 usec intervals. The sampling can be uniform or delayed by 4 usec between integrations. Integration of 1, 2, 4, or 8 sequences can be selected.

The Prober mode uses a 2047 bit PN sequence and is used to more accurately measure the channel. The transmitted pulse width is 1 usec with a 25% duty cycle. The received waveform is sampled at 4 usec intervals and sampling can be uniform or delayed by .5 usec between integrations of 1, 2, 4, or 8 sequences.

All data collection and processing parameters in the Portable Wideband HF Channel Analyzer are programmable and are set by software downloaded from the microcomputer. Parameters such as sequence length and sampling rate can be changed as long as they remain within the physical limitations of the system. The signal processors in the Portable HF Channel Analyzer are not limited to integration and correlation but can be programmed to perform other signal processing tasks as digital filtering and fast Fourier transforms (FFT's).

SECTION 2

Overview

The NRL0201 Digital Correlator is a digital signal processor designed by Stow Computer for the Naval Research Laboratory. The NRL0201 Digital Correlator was designed specifically for the Portable Wideband HF Channel Analyzer built by Stow Computer for NRL but could be used elsewhere as a digital correlator, FIR filter, or as a general purpose digital signal processor. The NRL0201 Digital Correlator interfaces to the Portable Wideband HF Channel Analyzer via the industry standard VMEbus. The VMEbus interface allows the NRL0201 Digital Correlator to be used in any microprocessor using the VMEbus.

Figure 1. is a block diagram of the NRL0201 Digital Correlator.

A Texas Instruments TMS320C25 digital signal processor is the central processing element of the NRL0201 Digital Correlator. The actual correlation is performed by an array of eight Motorola DSP56200 Finite Impulse Response digital filters in cascade. Dual-ported memories provide an efficient means of transferring data to and from the NRL0201 Digital Correlator. In addition to the 16k bytes of dual-ported memory there is memory internal to the TMS320C25 and the DSP56200's in the Correlator Array. TMS320C25 programs are generally stored internally after being loaded via the VMEbus. The IPB is a custom bus utilizing the user definable pins on the VMEbus J2 connector. The data memory ported to the IPB is always available to the TMS320C25 even if the NRL0201 Digital Correlator is installed in a backplane with no IPB connections.

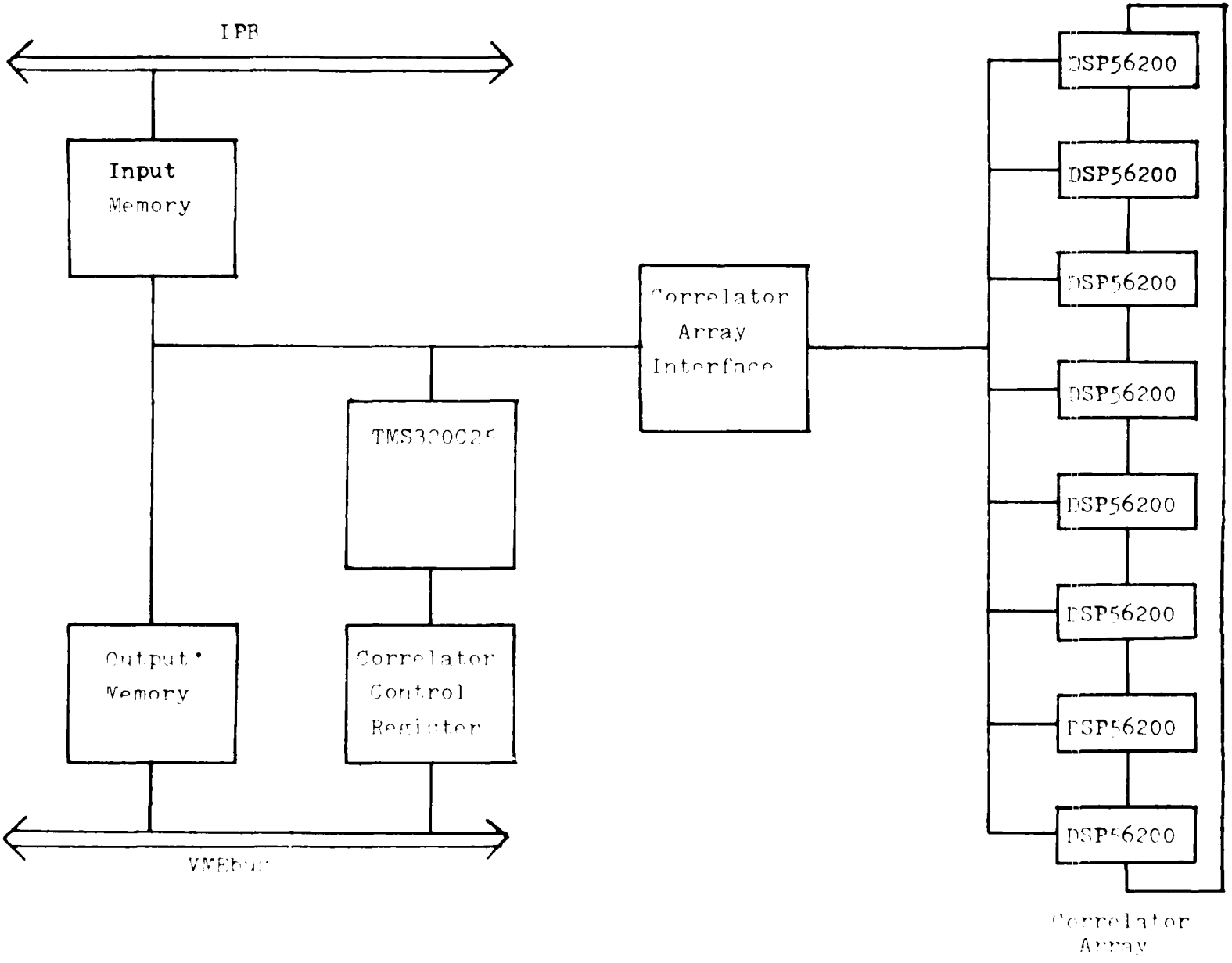


Figure 1. [illegible] Digital Correlator, Block Diagram

SECTION 3

TMS320C25 and Interface, Input and Output Memory TMS Ports

A Texas Instruments TMS320C25 digital signal processor is the central processing element of the NRL0201 Digital Correlator. The interface circuitry to the TMS320C25 comprises a clock circuit, address decoders and a circuit that generates READY. READY indicates to the TMS320C25 that an external read or write cycle is complete. The TMS320C25 stretches an external read or write cycle with wait states until READY is asserted. For maximum speed, the TMS320C25 address and data buses connect directly to the Input Memory, Output Memory and Correlator Array Interface latches, which are all high performance CMOS, without intermediate buffers. Most of the address decoding and the READY logic are combined into two programmable logic devices (PLD's). The clock input of the TMS320C25 is driven directly from a 40 mHz oscillator which also drives an octal flip-flop circuit used to generate 10 and 20 mHz processing clocks. These clocks have a fixed phase relationship and edges as close as possible to the internal TMS320C25 clocks.

Address decoding is simplified by not using the entire TMS320C25 address space. The Correlator Array is addressed by bit 15 (the MSB) of the address. Although this uses 32K bytes of the address space to address 129 registers, there is no decoding overhead. Address bits 14 and 13 of the TMS320C25 are not used externally and are effectively "don't cares" in the address decoding. These "don't care" bits are used to avoid some restrictions in the address space. The NRL0201 Digital Correlator uses the same physical memory in program space to download software and in data space as output memory. The program memory must start at location 0000 but data space addresses below 03FF (all addresses are shown in hexadecimal) are used internally in the TMS320C25. Adding an offset of 2000 to input memory references in the software makes the references external and, since bit 13 is not wired, physical memory receives addresses starting at 0000. TMS320C25 address decoding is shown in Table 1.

READY to the TMS320C25 is asserted based on a combination of address decoding and feedback from the device addressed. A read cycle to the Input Memory generates an immediate READY so that the TMS320C25 can proceed without wait states. When the NRL0201 Digital Correlator is operated in the Portable Wideband HF Channel Analyzer there should be no contention for access to the Input Memory. The BUSY signal from the Input Memory is connected to interrupt INT0 of the TMS320C25. This connection can be used to flag an exception to an Input Memory access if the NRL0201 correlator is programmed for a different application. Write

Bit 15	14	13	12	11	
1	x	x	x	x	Correlator Array
x	x	1	1		Output Memory 1
x	x	1			Output Memory 0
x	x	1	1		Input Memory 1
x	x	1			Input Memory 0

Table 1. Memory address decoding

cycles to the Correlator Array generate an immediate READY if ABUSY from the correlator array interface is not asserted. Software for the Portable HF Channel Analyzer is synchronized to the array so ABUSY will probably never cause wait states.

Read cycles accessing the Correlator Array have at least one wait state. The TMS320C25 cycle continues to stretch until RDRDY* is received from the Correlator Array Interface. Write cycles to either the Input or Output Memory have at least one wait state. This wait state allows the arbiter of the dual-ported memory to grant access or assert BUSY. If IBUSY or OBUSY is asserted the cycle stretches until the write can be completed. Read cycles accessing the Output Memory have at least one wait state in both data and program space. If OBUSY is asserted due to access from the VMEbus side, the TMS320C25 cycle stretches until the read can be completed.

SECTION 4

Correlator Array

The Correlator Array consists of eight Motorola DSP56200 Finite Impulse Response (FIR) Digital Filters in cascade. Each DSP56200 is a programmable length FIR filter with maximum length of 256 taps. The DSP56200 has an eight bit parallel interface used for loading data, coefficients, and control parameters and serial inputs and outputs for passing data and partial sums in the cascade. The autocorrelation function is performed by loading the coefficient memory of the FIR filter with a stored replica of the sequence being processed.

Eight DSP56200's in cascade are used to process a PN sequence of up to 2047 bits. The serial output of the last DSP56200 is connected to the serial input of the first to perform a circular shift of the data during the correlation. For details on the operation of the Motorola DSP56200 refer to the Motorola data sheet.

4.1 Correlator Array Interface

The Correlator Array Interface interfaces the Texas Instruments TMS320C25 digital signal processor, which functions as the central processor in the NRL0201 Digital Correlator, with the array of Motorola DSP56200 digital filters which perform the correlation. The Correlator Array is addressed as data memory by the TMS320C25. Address decoding is done by the TMS320C25 interface. The heart of the Correlator Array Interface is an Am29PL141 fuse programmable controller. This finite state machine sequences the interaction of the interface with the TMS320C25 and the DSP56200's. The Correlator Array Interface is optimized for transferring data from the TMS320C25 to the array. For highest performance the array must be loaded as quickly as possible. Correlator outputs from the array are spaced at the processing delay which allows plenty of time for the TMS320C25 to read the results.

The TMS320C25 writes sixteen bit data to the Correlator Array Interface. The DSP56200's used to perform the correlation have an eight bit interface. The Correlator Array Interface latches the data from the TMS320C25 so that the TMS320C25 can continue with no wait states and then performs two byte writes to the DSP56200 that was addressed. The TMS320C25 must not try to write to the Correlator Array in two consecutive cycles. When the Correlator Array is being loaded the TMS320C25 alternates between reading from the Input Memory and writing to the array. Thus, the

consecutive cycle restriction is not a problem and the pipeline is always full.

Data and addresses to the array are double buffered. Double buffering allows the TMS320C25 to initiate a write cycle while the previous write cycle is being completed. Addresses and data are also double buffered by the DSP56200 at its input port. The internal RAM memory of the DSP56200 is not directly accessed by the TMS320C25. The TMS320C25 writes an address to the RAM address register of the DSP56200 and, if it is a write cycle, writes data to the data register. These external registers are copied internally at the next START pulse. If a location of the internal DSP56200 RAM is being read, the read data is written to the external data register on the succeeding START pulse. DSP56200 cycles are shown in the Motorola data sheet. The START pulse is from the START Pulse Counter which is described below.

Output from the Correlator Array is read in bytes through the eight bit interface. The TMS320C25 must perform two read cycles and then combine the bytes into a sixteen bit word. The result of each correlation is stored in the output register of the last DSP56200 in the cascade and may be read by the TMS320C25 by addressing each byte of the output register. Reading data from the DSP56200's internal data RAM, however, is pipelined due to the double buffering. The data read on one cycle is from an address written into the address register on a previous cycle. Normal operation of the NRL0201 Digital Correlator in the Portable Wideband HF Channel Analyzer does not require reading the DSP56200's internal data RAM.

Write cycles from the TMS320C25 to the array are performed in a single cycle with no wait states. When the TMS320C25 reads the array, however, several cycles are required and the cycles accessing the array are stretched by wait states. The difference in performance between reads and writes is a result of the optimization of the design. In the Portable Wideband HF Channel Analyzer the time spent writing to the array impacts performance. There is ample time to read the output of the Correlator Array.

Operations supported by the Correlator Array Interface are: read even byte, read odd byte, word write, write odd byte, and write to the modulus register of the START Pulse Counter. Read even byte reads the register at the even address specified and places the data on D07 through D00. Read odd byte reads the register at the odd address specified and places the data on D07 through D00. Word write writes the LSB of the data from D07 through D00 into the register at the even address specified plus one then writes the MSB of the data from D15 through D08 into the register at the address specified. Write odd byte writes

the LSB of the data from D07 through D00 into the register at the odd address specified. Write to START Pulse Counter modulus register writes the MSB of the data from D15 through D08 to the modulus register of the START Pulse Counter. Note that it is the MSB that is transferred. The START Pulse Counter is described in section 4.2.

These operations are defined to interface the TMS320C25 which does only word transfers with the DSP56200 which does only byte transfers. The Correlator Array Interface determines the type of operation from the read/write signal and the LSB of the address from the TMS320C25. It then performs one or more operations to complete the desired transfer. The LSB of the DSP56200 register address is generated by the interface. For example, when the TMS320C25 writes to an even location (word write), the interface first does a write to the odd byte then the even byte. Byte writes to odd bytes were included because the control registers of the DSP56200 are at odd byte addresses. The modulus of the START Pulse Counter is set using the most significant byte of the data because it was easier to implement in the hardware than if the least significant byte were used.

4.2 START Pulse Counter and START Pulse Counter Modulus Register

The START Pulse Counter generates the synchronous START pulse required by the DSP56200. The period of the START pulse is equal to the filter length plus some overhead as defined in the DSP56200 data sheet. The START pulse is used to transfer data that is double buffered in the DSP56200 into and out of the interface registers. While the Correlator Array is being loaded with data, the filter length is set to the minimum value so that START can occur at the maximum frequency for fastest loading. The period of the START pulse is set through the START Pulse Counter modulus register. The START Pulse Counter circuitry also generates a gating pulse, SWRN, which inhibits the initiation of transfers to or from the TMS320C25 for a period around the START pulse. This period was determined by adding the required dead time from the DSP56200 data sheet to the time for the microcode of the longest transfer to complete.

The START Pulse Counter modulus register is loaded from the most significant byte of the data bus and determines the period of the START pulse. The START Pulse Counter is a 9-bit counter clocked by the same 10 mHz clock as the Correlator Array. The value loaded into the register is the determined by writing the period determined from the DSP56200 data sheet as a 9-bit binary number, subtracting one, taking the one's complement, and shifting the eight MSB's to the most significant byte of a 16-bit number.

Normal values for the start pulse counter modulus are listed in Table 2.

Total Number of Taps	START Pulse Period	Modulus Register Value
32	49 x 100ns	E700
256	49 x 100ns	E700
2048	267 x 100ns	7A00

Table 2. Typical Values for START Pulse Counter Modulus Register

SECTION 5

IPB Interface and Input Memory IPB Port

The Inter-processor Bus or IPB is used to transfer data between the Analog to Digital Converter, Integrator, and two NRL0201 Digital Correlators in the Portable Wideband HF Channel Analyzer. The IPB specification is based on the VMEbus VMX subsystem bus. Signal timing, driver and receiver specifications are taken from the VMXbus specifications. The IPB is optimized for the Portable Wideband HF Channel Analyzer. The IPB has 13 non-multiplexed address lines, 32 data lines, an address strobe, data strobe and a read/write control line. Link signals allow the two correlators in the Portable Wideband HF Channel Analyzer to operate as a single slave device. The NRL0101 Integrator is always the IPB master. The 32 data lines are utilized as two 16 bit channels. Each correlator operates on one channel (in-phase or quadrature data) which is selected by installing the bus transceivers for the desired channel.

5.1 Configuring the IPB Port

The NRL0201 Digital Correlators are configured for linked operation on the IPB by DIP switch DS1. DS1 SW1 when closed (on) configures the NRL0201 Digital Correlator to generate IPB ACK*. If DS1 SW1 is open (off) the correlator generates LINKOUT* which is a synchronization signal to the correlator generating ACK*. DS1 SW2 when closed (on) causes the correlator to wait for LINKIN* before generating ACK*. The normal configuration for the two correlators in the Portable Wideband HF Channel Analyzer is for one correlator to wait for LINKIN* and generate ACK* (DS1 SW1 on, SW2 on) and the other correlator to generate LINKOUT* (DS1 SW1 off, SW2 off). The correlator generating ACK* must be in the higher numbered of two adjacent slots in the backplane. LINKOUT* and LINKIN* use the SMACKOUT* / SMACKIN* connections of the VMX backplane.

NRL0201 Digital Correlators are configured for the in-phase or quadrature (I or Q) channel by the installation of one pair of 74F245 bus transceivers. Transceivers are installed in positions U14 and U15 for in-phase data or in positions U28 and U29 for quadrature data.

5.2 Input Memory

Transactions over the IPB go directly to the correlator Input Memory. The Input Memory is an 8K byte dual-ported memory. One port connects to the IPB interface, the other to the TMS320C25. Operation of the memory ports is

independent unless both ports try to access the same location simultaneously. If both ports try to access the same location an internal arbiter grants access to one port and delays access to the other port by asserting BUSY*. In the Portable Wideband HF Channel Analyzer the correlator input memory is operated as two 2k word buffers. One buffer is used by the NRL0101 Integrator as data memory as input samples are collected while the TMS302C25 unloads the other buffer. The buffers exchange roles by mutual agreement between the Integrator and the TMS320C25 using a mailbox scheme.

SECTION 6

VMEbus Interface

The NRL0201 Digital Correlator is fundamentally a VMEbus based digital signal processor. The VMEbus is an international interconnection standard. The NRL0201 Digital Correlator conforms to the VMEbus specification REV C.1 in terms of signal definition, timing, dc loading, and drive capability. The capacitive loading of a several signals may exceed the specification by a few pico-farads. The NRL0201 Digital Correlator is a VMEbus SLAVE with A16, A24, D08(EO), and D16 capability. This means that the correlator will not initiate transfers but will respond to 16-bit (short) or 24-bit (standard) addressing and can transfer data in bytes (both even and odd) or in 16-bit words.

The User-Defined pins of the VMEbus J2 connector are used in the Portable Wideband HF Channel Analyzer to implement an inter-processor bus (IPB), a control bus, and for signals that allow two NRL0201 Digital Correlators to be linked in order to occupy the same VMEbus address space and transfer data to the system microcomputer in 32-bit longwords (D32). In the Portable Wideband HF Channel Analyzer this capability is used to process the in-phase and quadrature channel data from the Digital Pre-processor in parallel and make use of the bandwidth of a 32-bit data bus in transferring tap gains to the system microcomputer.

The NRL0201 Digital Correlator can be used without modification in a standard VMEbus system if no connections are made to rows A and C of connector J2. A configuration switch on the NRL0201 Digital Correlator shifts the addresses of the on-board memory and control register so that two correlators can be used in the same VME backplane without modification. Thus, although designed specifically for the Portable Wideband HF Channel Analyzer, the NRL0201 Digital Correlator can perform correlation and other signal processing tasks in a pure VME environment.

6.1 VME Interface Configuration Switches DS2

A dual DIP switch, DS2, configures the VMEbus interface of the NRL0201 Digital Correlator. Switch SW1 of DS2 selects stand-alone or linked mode. When SW1 is closed (on) the VMEbus interface operates in stand-alone mode and generates the VMEbus acknowledgement signal DTACK* in response to being addressed. When SW1 is open (off) the VMEbus interface operates in co-operation with another NRL0201 Digital Correlator in the backplane. The signals generated by the interface in linked mode depend on the setting of switch SW2 of DS2. The correlator having SW2

closed (on) generates VLINKOUT* instead of DTACK* in response to being addressed. Data transfers from this correlator are routed over D31 through D16 on the data transfer bus. The correlator with SW2 open (off) waits for VLINKIN* before generating DTACK* and transfers data over D15 through D00. VLINKOUT* and VLINKIN* are connected on the backplane.

SW2 is used in stand-alone mode to shift the base addresses of the Correlator Control Register and Output Memory. If SW2 of DS2 is closed (on) in stand-alone mode the base address of the correlator Output Memory is shifted up by 8k bytes and the address of the Correlator Control Register is shifted up by two bytes to allow another correlator with SW2 off to operate in the same backplane. Operation of DS2 is shown in Table 3. The VMEbus addresses, Correlator Control Register, and Output Memory are described in the following sections.

6.2 VMEbus Addresses

The VMEbus addresses used in the Portable Wideband HF Channel Analyzer for the correlator Output Memory are FF4000 through FF7FFF. The 16k bytes of address space are required for the Output Memories of the two linked NRL0201 Digital Correlators. The linked output memories are used as two 2k by 32-bit buffers to transfer I and Q channel data in parallel. Addresses FFFF10 - FFFF13 on the VMEbus are used for the Correlator Control Registers. The Correlator Control Registers of the two NRL0201 Digital Correlators are accessed in parallel by 32-bit transfers initiated by the system microcomputer. The VMEbus addresses used by the NRL0201 Digital Correlator may be changed by programming new programmable logic devices (PLD's). For two correlators operating in linked mode on the VMEbus 16 kbytes of address space starting on a longword boundary are required for the Output Memories and four bytes starting on a longword boundary are required for the Correlator Control Registers.

Valid AM (Address Modifier) codes for accessing the Output Memory or Correlator Control Registers are:

3D Standard Supervisory Data Access
39 Standard Non-privileged Data Access
2D Short Supervisory Data Access
29 Short Non-privileged Data Access

User definable codes may be programmed into the PLD's if required. Other AM codes are either not supported or do not make sense.

SW1	SW2	Mode	Data	Base Addresses
0	0	Linked, Generate DTACK*	D15-D00	FF4000 Output Memory FFFF10 Corr. Control
0	1	Linked, Generate VLINKOUT*	D31-D16	FF4000 Output Memory FFFF10 Corr. Control
1	0	Stand-Alone Generate DTACK*	D15-D00	FF4000 Output Memory FFFF10 Corr. Control
1	1	Stand-Alone Generate DTACK*	D15-D00	FF6000 Output Memory FFFF12 Corr. Control

Table 3. VMEbus Configuration Switch (DS2) Settings

6.3 Correlator Control Register

The Correlator Control Register (CCR) is an eight bit register. The Correlator Control Register is written and read over the VMEbus. Only three bits of the register are used. Reading the Correlator Control Register over the VMEbus is primarily intended for diagnostic use but may be used by the system microcomputer as required.

The two NRL0201 Digital Correlators in the Portable Wideband HF Channel Analyzer operate in linked mode on the VMEbus. The correlator configured as upper by SW2 of DS2 has its Correlator Control Register mapped to VMEbus data bits D31 through D24. The correlator not configured as upper has its Correlator Control Register connected to data bits D15 through D08. The Correlator Control Registers of both correlators are accessed with a single longword transfer from the system microcomputer. It is anticipated that the Correlator Control Registers of both correlators will be written with identical data but this is not a requirement. Also, care must be taken that there is valid data for both bytes 0 and 2 before the longword transfer is made. Otherwise, for example, one correlator could be inadvertently interrupted or reset.

If two correlators are in the same VME backplane but are not configured as linked, one must be configured as upper and one not. The Correlator Control Register of the NRL0201 Digital Correlator configured as upper is at address FFFF1[illegible] and may be accessed by a word or byte transfer using data lines D15 through D08. The Correlator Control Register of the correlator not configured as upper is at address FFFF1[illegible], also uses data lines D15 through D08 and may be accessed by a word or byte transfer.

The control bits are D15 (D31) RESET*, D09 (D25) INT1*, and D08 (D24) BIO* where "*" means that the signal is active low and is asserted by writing a "0" into the register at that bit position. Numbers in parentheses refer to a correlator operating in linked mode and configured as upper. RESET* causes a hardware reset of the TMS320C25 and the Correlator Array. INT1* is the TMS320C25 level 1 interrupt. INT1* is both edge and level sensitive. BIO* is the TMS320C25 branch control input. This signal may be polled by the TMS320C25 using the BIOZ instruction. Refer to the TMS320C25 manual for details on interrupts, BIO* and BIOZ.

6.4 Output Memory VME Port

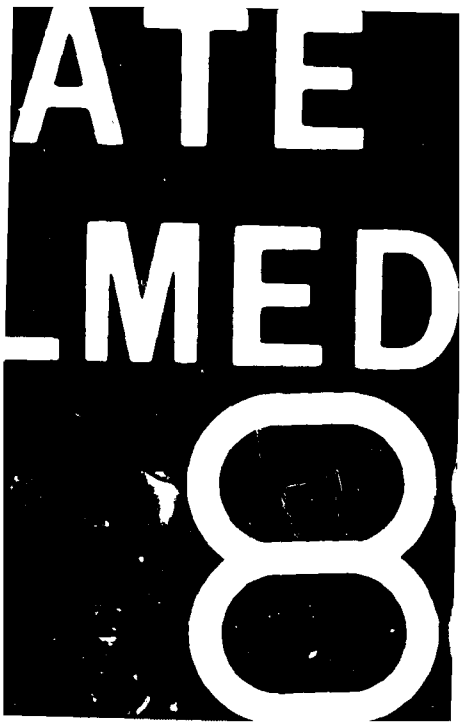
The Output Memory serves as both a data memory for the output of the NRL0201 Digital Correlator and as program memory for downloading software to the correlator. The Output Memory is an 8K byte dual-ported random access memory (RAM). The VME and TMS320C25 ports of the memory operate

completely independently except when each side tries to access the same address. If both ports try to access the same address simultaneously an internal arbiter grants access to one port and delays access to the other port by asserting BUSY*. Arbitration should not be required during normal analyzer operation because the output memory of each correlator is divided into two 2K by 16-bit buffers with the correlator and system microcomputer switching buffers by mutual agreement using a mailbox scheme.

The output memories of both correlators in the Portable Wideband HF Channel Analyzer are accessed simultaneously in linked mode by the system microcomputer using a common address. Data is transferred in 32-bit longwords. The correlator configured as upper by SW2 of DS2 transfers data over D31 through D16. The other correlator transfers data over D15 through D00. Since data is transferred only in longwords, programs must be simultaneously loaded into both correlators with the instructions for the correlator configured as upper in the two most significant bytes. Normally the same program would be loaded into both correlators but this is not a requirement.

The correlators do not have to be configured in linked mode. A correlator can operate on the VMEbus in stand-alone mode. In stand-alone mode all data transfers are on data lines D15 through D00 and data may be transferred in either words or bytes. Unless it is configured as upper by SW4 of S4, the output memory of a correlator in stand-alone mode occupies the VMEbus address space from FF4000 through FF5FFF. Two correlators may be operated in stand-alone mode on the same VME backplane by configuring one as upper using SW4 of DS2. The output memory of a correlator configured as stand-alone and upper is addressed from FF6000 through FF7FFF.

The IMS T425 architecture reserves the first 32 locations of program memory for interrupt vectors. Thus, 32 locations of the common program and data memory at one of the output buffers is not available for data storage. Correlator output that would otherwise be stored in these locations is stored internally in the IMS T425 and is retrieved when requested by an interrupt from the system microcomputer.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